

Coupling Between Microstrip Lines With Finite Width Ground Plane Embedded in Thin Film Circuits

George E. Ponchak, Edan Dalton, Manos M. Tentzeris, and John Papapolymerou

Abstract-- Three-dimensional (3D) interconnects built upon multiple layers of polyimide are required for constructing 3D circuits on CMOS (low resistivity) Si wafers, GaAs, and ceramic substrates. Thin film microstrip lines (TFMS) with finite width ground planes embedded in the polyimide are often used. However, the closely spaced TFMS lines are susceptible to high levels of coupling, which degrades circuit performance. In this paper, Finite Difference Time Domain (FDTD) analysis and experimental measurements are used to show that the ground planes must be connected by via holes to reduce coupling in both the forward and backward directions. Furthermore, it is shown that coupled microstrip lines establish a slotline type mode between the two ground planes and a dielectric waveguide type mode, and that the via holes recommended here eliminate these two modes.

Index terms—microstrip, coupling, crosstalk, FDTD

I. INTRODUCTION

Demand is growing for Microwave Monolithic Integrated Circuits (MMICs) and packaged MMICs with greater functionality, lower cost, and smaller size. Furthermore, the digital processing and control functions of the system are now often incorporated into the same package as the analog circuits and MMICs. However, consumer, military, and aerospace components must fit into smaller areas. Thus, two-dimensional packages are no longer suitable for many of these applications. Instead, three-dimensional (3D) packages and integration technologies are required.

A widely used, low cost technology that is currently used for packaging individual circuits and integrated systems is Low Temperature Cofired Ceramic (LTCC). By laminating multiple layers of thick (0.1-0.15 mm) ceramic sheets with thick film metal lines on each layer and metal filled via holes to interconnect the various layers, complex 3D circuits are possible [1-3]. An alternative multi-layer packaging technology is commonly called Multi-Chip Module-Deposited (MCM-D) [4-6] or High Density Interconnect (HDI) [7] that consists of multiple layers of thin film polyimide deposited onto a ceramic carrier. Portions

of a thin film metal circuit are fabricated on each layer of polyimide and interconnected by etched via holes. MMICs and Integrated Circuits (ICs) may be attached to the upper polyimide layer after the final layer is deposited, or they may be placed in wells etched into the ceramic carrier. Instead of thin, deposited polyimide layers on ceramic and flip chip or wire bonded circuits, higher levels of integration and circuit variability are possible by depositing polyimide directly onto GaAs [8,9] and Si [10,11] substrates with all of the circuitry monolithically fabricated on the same wafer. In this way, passive circuit components, which occupy most of the area of ICs and MMICs, and antennas may be placed over the active circuits that are fabricated on the semiconductor. Another advantage of thin film polyimides on Si is that microwave passive elements and transmission lines placed directly on standard CMOS and BiCMOS grade Si, which have resistivities of 1 and 20 Ω -cm respectively, have low quality factors (high attenuation), which necessitates novel transmission line structures [12] that are typically embedded in the polyimide.

Achieving sufficient isolation between transmission lines embedded in multi-layer substrates is critical for proper circuit/system performance. However, when transmission lines are close together, direct coupling between them is high, and in multilayer circuits where transmission lines may be under each other, the coupling is even higher [13]. In addition to direct coupling, transmission lines on isotropic and anisotropic substrates may excite surface waves on the substrate that will leak power away from the excited line and couple it to other lines on the substrate. It has also been shown that these leaky, surface wave modes may have an electromagnetic field distribution that resembles the field distribution of a microstrip line near the line [14]. Thus, it is easily excited in circuits.

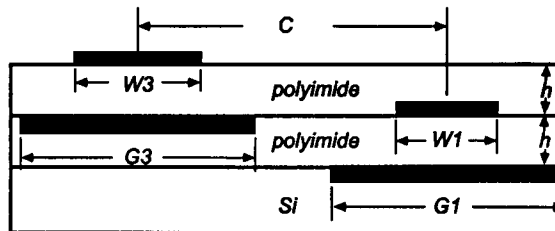
A commonly used transmission line in these multi-layer circuits and packages is microstrip or, as it is called when implemented on thin films, Thin Film Microstrip (TFMS). When used on Si CMOS and BiCMOS circuits, the ground plane shields the electromagnetic fields from the lossy Si [12], which provides a low loss transmission line. Coupling between microstrip lines with infinite ground planes built on Low Temperature Cofired Ceramic (LTCC) [15] and embedded in polyimide [16,17] with shielding structures built into the substrate have been thoroughly characterized. However, in many of these 3D circuits and packages, a finite width ground plane is used to enable higher levels of integration, and on LTCC packages where a high percentage of the ceramic must be open to ensure ceramic bonding and control shrinkage, finite width ground planes are required. TFMS with finite width ground planes has a higher loss than conventional microstrip lines, but, if the ground plane is greater than 3 to 5 times the strip width, acceptable attenuation is achieved [18]. Also, by reducing the ground plane width, ground planes may be placed on different layers to give another design option. For example, antenna radiation characteristics are modified by changing the ground plane dimensions of microstrip patch antennas [19]-[21].

Coupling between finite width ground plane microstrip lines embedded in polyimide has been experimentally investigated [22]. However, [22] raised questions about parasitic modes that could not be answered experimentally. In this paper, an analysis of the coupling between TFMS lines with finite width ground planes embedded in polyimide built upon CMOS grade Si is presented. This analysis includes a comparison of the coupling between transmission lines built on different layers of polyimide, and the use of metal filled via posts to connect ground planes on different layers. An emphasis is placed on a Finite Difference Time Domain (FDTD) analysis of the lines to understand the parasitic modes and their role in the coupling characteristics.

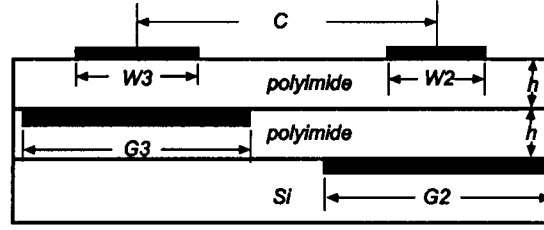
II. CIRCUIT DESCRIPTION

Fig. 1 shows a cross sectional cut through two variations of microstrip lines embedded in polyimide upon a Si substrate. TFMS lines are characterized with ground plane widths of 3 and 5 times the strip width. W_1 , W_2 , and W_3 are 23 μm , 52 μm , and 25 μm respectively to yield 50 Ω transmission lines for the polyimide thickness, h , of 10 μm . As was proposed in [22] and will be expanded upon here, there is an advantage to connecting the two ground planes. Thus, in several coupled microstrip lines and in the FDTD analysis, the two ground planes on different layers are connected by a single row of 20 μm by 20 μm via holes spaced 100 μm apart, which is a via spacing less than one hundredth of a wavelength at 25 GHz. To accomplish this when the ground planes did not overlap, the ground planes were extended in one direction so that they overlapped by 20 μm . The parameter C is the distance between the centerlines of the two TFMS lines.

For the experimental characterization, a four-port circuit is used for measuring the coupling between the microstrip lines with probe pads orientated so that each port may be probed simultaneously with the port numbering as shown in Fig. 2. The 90 degree bends are not required for the FDTD analysis. The coupling region, or the section of parallel transmission lines labeled L in Fig. 2, is 5000 μm long for the experimental characterization, but the coupling length was varied from 3000 to 5000 μm for the FDTD analysis. While these are physically short lines, they have an electrical length between 180° and 270° at 25 GHz, which is required for rat-race, hybrid, and Wilkinson dividers. Longer lines, which would have higher coupling, would be required for antenna feed networks.



(a)



(b)

Figure 1: Cross sectional cuts through microstrip lines with finite width ground planes embedded in polyimide layers (a) microstrip lines with same substrate thickness (b) microstrip lines with different substrate thickness.

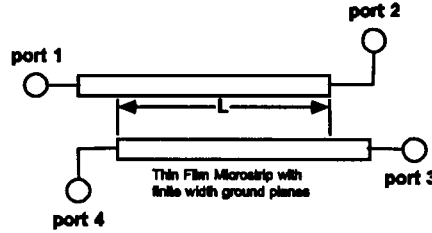


Figure 2: Schematic of the four-port microstrip line structure used to characterize coupling experimentally. The same port designations used in the FDTD analysis.

III. THEORETICAL ANALYSIS

The full-wave FDTD technique [23] is used for the theoretical characterization of the forward and backward coupling, S_{31} and S_{41} respectively, between the two parallel microstrip lines. The E- and H-field components are implemented in a leapfrog configuration. An adaptive grid with neighboring cell aspect ratio smaller or equal to 2 maintains a second-order global accuracy.

Numerical meshes of 80-120 by 45 by 250 cells terminated with 10 Perfectly Matched Layer (PML) cells in each direction provide accurate results for a time-step of $\Delta t = 0.99 \Delta t_{\max}$. A Gaussian pulse with $f_{\max} = 60$ GHz is applied vertically as a soft source close to the front end of the microstrip, and its values get superimposed on the FDTD calculated field value for all cells in the excitation region for each time-step. The via holes are modeled as rectangular metal tubes with cross-section $23 \times 20 \mu\text{m}$. To account for the excitation of different modes in the microstrip lines, two simulations are performed for each geometry exciting both lines with equal amplitude and even or odd space distributions respectively. In addition, both microstrip lines are terminated with matched loads ($Z_0 = 50 \Omega$) that are realized as the combination of shunt resistors placed between the microstrip and the bottom ground [24]. Probes placed at the front end and at the far end of one line are used for the combination of the

results of the even and of the odd simulations. The application of the FFT algorithm derives the frequency-domain results from the time-domain data (usually 20,000 time-steps).

As will be seen in a later section, multiple modes propagate along the coupled line. Therefore, to assure that the microstrip mode characteristics are being measured, two probes, equally spaced to the left and right of the center of the microstrip line are used and the average of those two probe voltages yields the microstrip mode voltage.

IV. CIRCUIT FABRICATION AND CHARACTERIZATION

The four port microstrip circuits are fabricated on a 1 Ω -cm Si wafer. The lowest level ground plane consisting of a 300 Å Ti adhesion layer, 1.5 μ m of Au, and a 200 Å Cr cap layer is first evaporated onto the Si wafer. Then, Dupont adhesion promoter and 10 μ m of Dupont PI-2611 polyimide, which has a relative dielectric constant, ϵ_r , of 3.12 measured at 1 MHz [25] and a loss tangent of 0.002 measured at 1 kHz [26], is spun onto the wafer. After curing the polyimide at 340 C for 120 minutes, a Ni mask is evaporated and patterned on the polyimide for the O_2/CF_4 reactive ion etching (RIE) of the via holes. After the via holes are etched and the Ni removed, 200 Å of Ti and 2000 Å of Au are sputtered onto the wafer to serve as a seed layer for the 1.3 μ m of Au electroplating that is used to define the embedded microstrip lines and fill the via holes in a single step. This Au is capped with 200 Å of Cr before applying the next layer of polyimide. Thus, all metal structures are 1.5 μ m thick. This process is repeated for each layer of polyimide. A DEKTAK surface profile and an SEM analysis of the polyimide and metal strips show that the surface roughness is low enough that it can be neglected in the analysis.

Measurements are made on an HP8510C vector network analyzer from 1 to 50 GHz. A Thru/Reflect/Line (TRL) calibration is implemented with MULTICAL [27], a TRL software program, using four delay lines of 1800, 2400, 4800, and 10000 μ m and a short circuit reflect fabricated on the same substrate as the circuits. To improve accuracy, each circuit is measured several times and the average of those measurements is presented in this paper. Two of the four ports are terminated in 50 Ω loads built into especially designed RF probes during testing of the coupling circuits.

V. MICROSTRIP CHARACTERISTICS

The measured effective permittivity, ϵ_{eff} , and attenuation of the microstrip lines embedded in polyimide are shown in Fig. 3. It is seen that for $f < 40$ GHz, lines of width W1 and W3, which have nearly identical width, have similar attenuation, and the microstrip line with width W2, which uses the entire polyimide thickness for its substrate, has lower loss. However, above 40 GHz, the loss of the wider line on the thicker substrate is higher. This is probably due to higher radiation loss for the wider microstrip line. The effective permittivity of the completely embedded line, W1, is equal to the relative permittivity of the polyimide at high frequency.

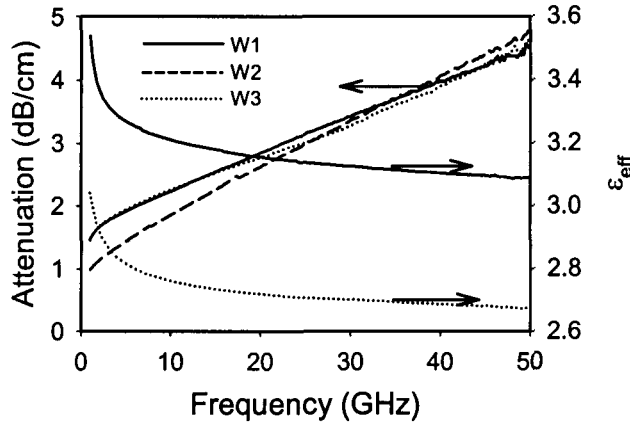


Figure 3: Measured attenuation and effective permittivity of microstrip

lines embedded in polyimide.

VI. MICROSTRIP COUPLING

The measured and FDTD analysis results for the embedded microstrip lines are compared across the frequency band of 1 to 50 GHz for a typical case in Fig. 4. There is very good agreement with a maximum difference of 3 dB. Thus, conclusions from either technique may be assumed to be correct. Throughout the paper, the forward coupling is defined as $-20\log|S_{31}|$ and the backward coupling is $-20\log|S_{41}|$. Measured forward and backward coupling of TFMS lines is summarized in Fig. 5a and 5b respectively. It is seen that coupling decreases nearly linearly as C increases, decreases by 3 to 5 dB as the ground plane increases from 3 to 5W, and is 3 to 5 dB lower for the coupled TFMS of Fig. 1a. Thus, to improve isolation, a wider ground plane and thinner microstrip substrates are desirable. Note that these results are for widely spaced transmission lines ($C/h > 5$).

Returning to Fig. 4, it is noted that $|S_{31}|$ increases monotonically with frequency, but it does not increase smoothly as is typical of coupling between two TEM transmission lines [28] and coupled microstrip lines [17]. Backward coupling, $|S_{41}|$, of two TEM transmission lines should have a series of maxima of the same magnitude and a periodicity dependent on the coupling length, L . However, as seen in Fig. 4, $|S_{41}|$ has a periodic frequency dependence and a component that increases monotonically with frequency. Both of these characteristics is an indication that there are two components of coupling, direct coupling and indirect coupling through phantom circuits or, as they are now commonly called, parasitic modes [28]. This is not surprising because the coupled, finite width ground plane microstrip lines shown in Fig. 1 have four metal lines, which supports three independent TEM modes if the media was homogeneous. In addition, because the 3D-circuits consist of layers of low permittivity material over the higher permittivity Si, slab waveguide/dielectric waveguide modes are possible. Thus, indirect coupling through phantom circuits is expected.

To reduce the number of modes, the two ground planes may be connected with via holes. It may be surmised that a coupled strip or slotline type mode propagates along the two coupled ground planes, and this mode is shorted by the metal interconnects.

In [22], it was experimentally shown that connecting the two ground planes reduces coupling by 5 dB for a 5000 μm long coupled line section. FDTD analysis of 3000 μm long coupled lines, which is shown in Fig. 6, shows that the via posts reduces the effects of the parasitic modes. Note that $|S_{41}|$ is now periodic with frequency and $|S_{31}|$ increases smoothly with frequency for both cases (Fig 1a and Fig 1b).

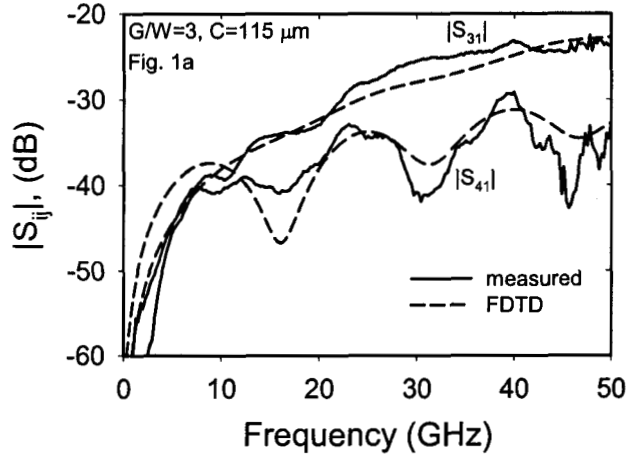
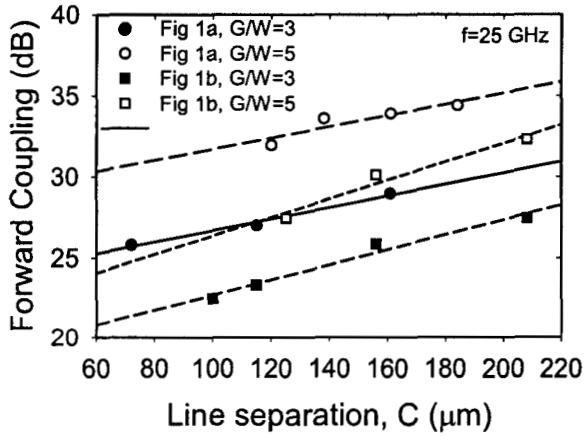
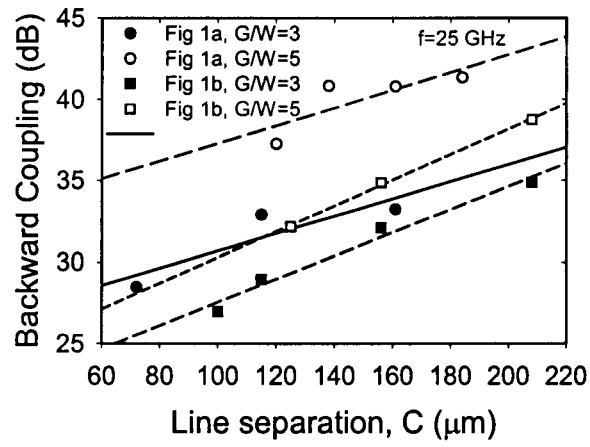


Figure 4: Measured and FDTD analysis S-parameters for coupled

microstrip lines with the same substrate thickness (Fig. 1a) and $L=5000 \mu\text{m}$ as a function of frequency.

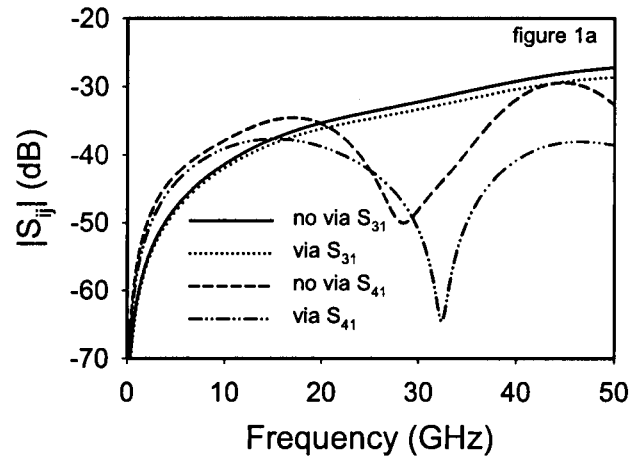


(a)

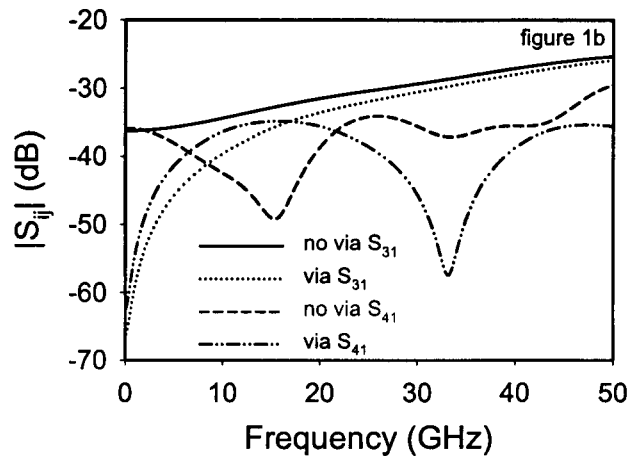


(b)

Figure 5: Measured (a) forward and (b) backward coupling of coupled microstrip lines of Fig.1a and Fig 1b at 25 GHz and $L=5000 \mu\text{m}$.



(a)



(b)

Figure 6: FDTD analysis determined S-parameters for $C=115\ \mu\text{m}$, $L=3000\ \mu\text{m}$ and (a) structure of Fig. 1a, and (b) structure of Fig. 1b.

VII. ELECTROMAGNETIC FIELDS OF COUPLED LINES

While the measured and FDTD analysis coupling characteristics, $|S_{31}|$ and $|S_{41}|$, support conclusions that connecting the ground planes of microstrip lines with finite width ground planes greatly decreases coupling and eliminates or reduces the magnitude of parasitic modes, this conclusion has not been proven. FDTD analysis is capable of mapping the electric and magnetic fields of coupled microstrip lines and separating them into the various modes by using cross-sectional probes for specific frequencies and identifying the differentiating features of the different modes. Figures 7 through 10 show the electric and magnetic fields for two cases of coupled lines shown in Fig. 1 both with and without via posts. The electric fields for the lines without via posts shown in Figs. 7a and 9a show high fields between the ground plane and silicon substrate of the coupled line. Similarly, Figs. 7b and 9b show there are high magnetic fields between the ground planes of two microstrip lines. Lastly, the electric fields under the coupled line and between the ground planes are stronger for the coupled lines shown in Fig 1b. With the via posts, the fields between the two ground planes are completely eliminated, and the electric field under the ground plane of the coupled line is reduced. The effect is more prominent for larger spacing C between the lines ($C=115\ \mu\text{m}$ vs. $C=92\ \mu\text{m}$) that allows for the easier excitation of the slotline mode between the grounds. These qualitative observations indicate two parasitic modes: the first is a dielectric waveguide type mode and the second is a slotline type mode between the two ground planes. The via posts reduce or eliminate both of these modes.

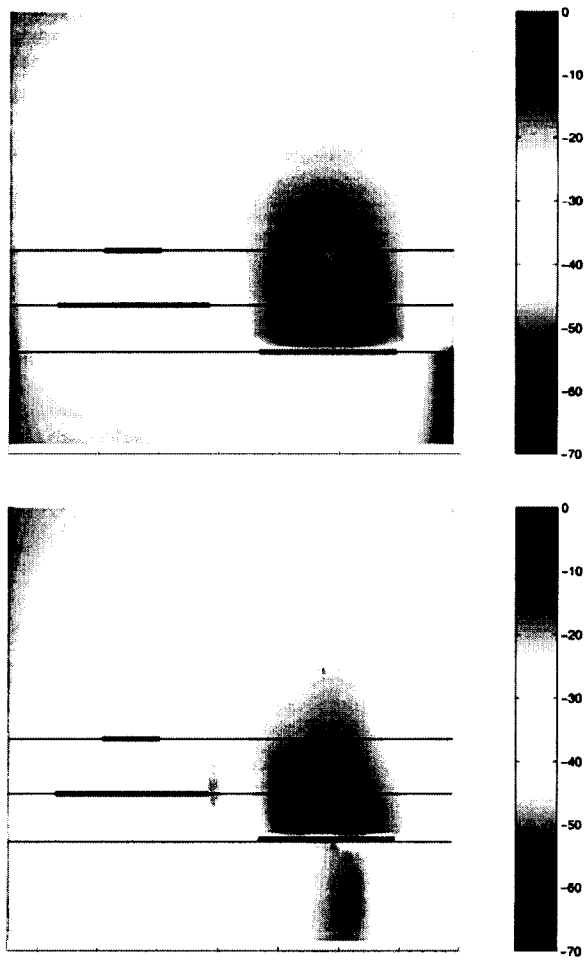


Figure 7: FDTD derived (a) electric and (b) magnetic field plots for coupled microstrip lines shown in Fig 1a without via posts at 20 GHz and $C=92\ \mu\text{m}$.

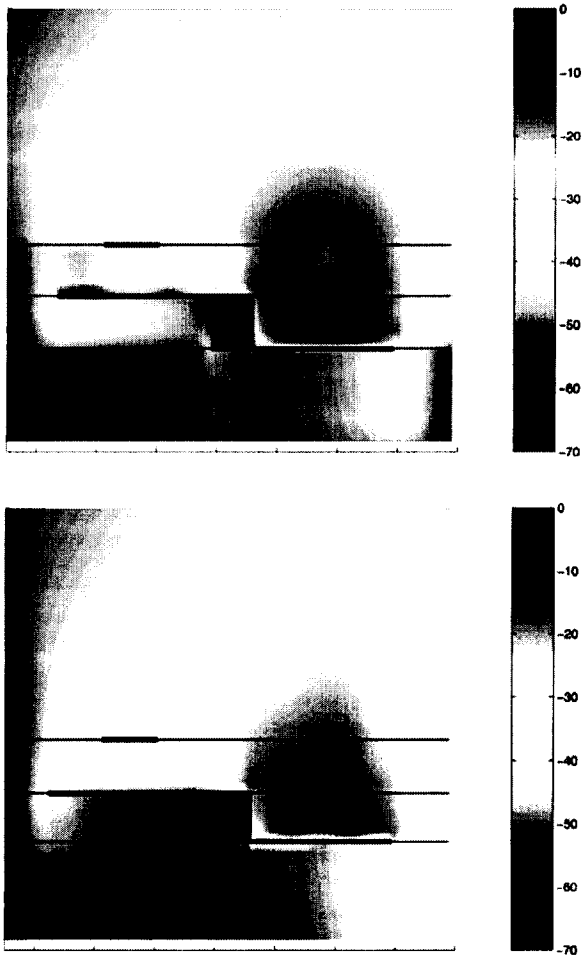


Figure 8: FDTD derived (a) electric and (b) magnetic field plots for coupled microstrip lines shown in Fig 1a with via posts at 20 GHz and $C=92\ \mu\text{m}$.

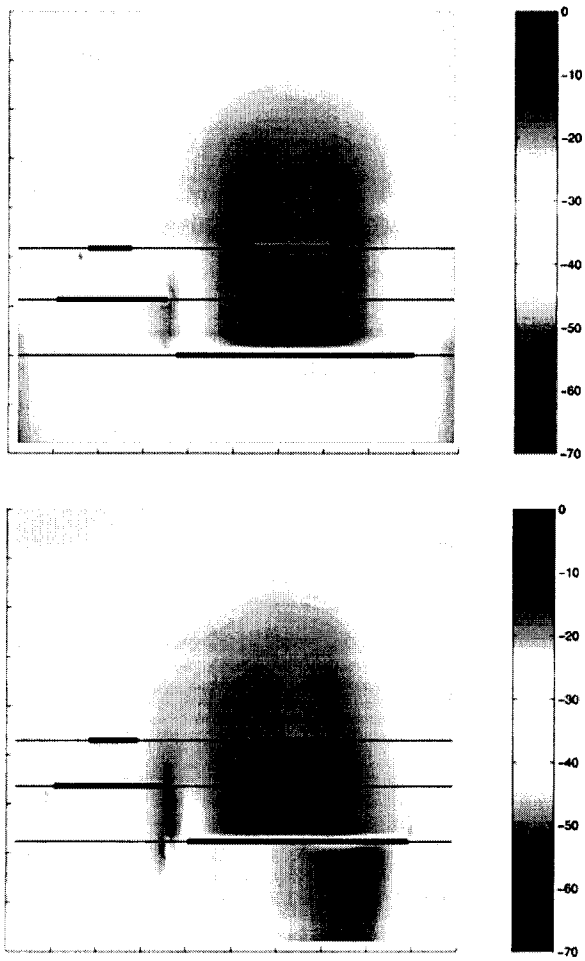


Figure 9: FDTD derived (a) electric and (b) magnetic field plots for coupled microstrip lines shown in Fig 1b without via posts at 20 GHz and $C=115\ \mu\text{m}$.

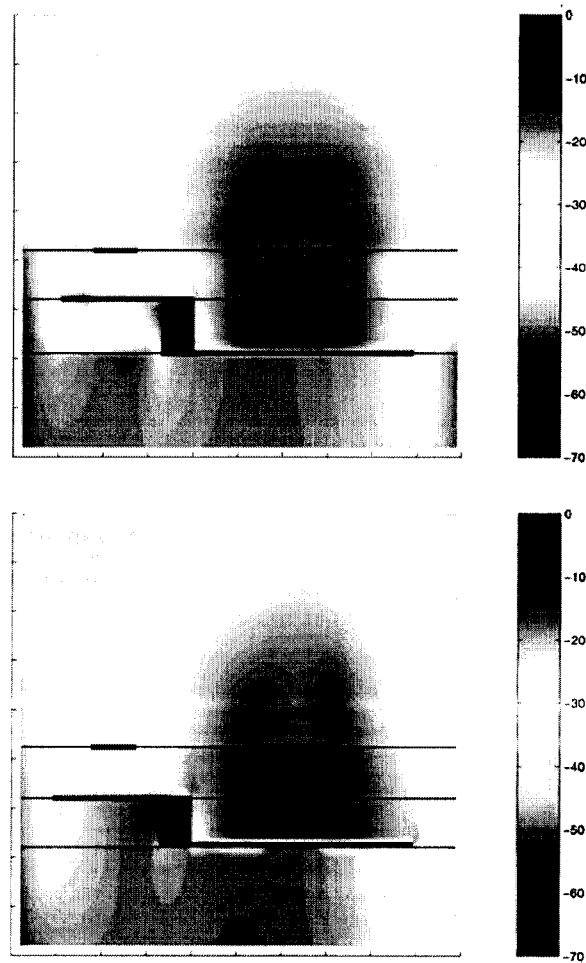


Figure 10: FDTD derived (a) electric and (b) magnetic field plots for coupled microstrip lines shown in Fig 1b with via posts at 20 GHz and $C=115\ \mu\text{m}$.

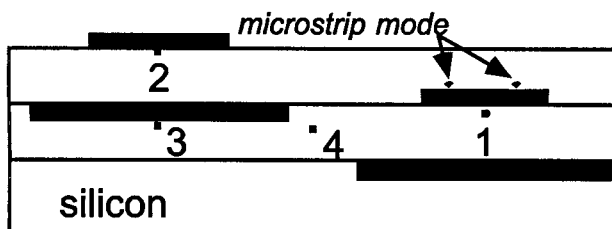


Figure 11: Probe locations for determination of coupled microstrip modes. Probes 1 and 2 are the average of two probes spaced equal distant from center of line as shown above right hand side microstrip. Probe 4 is equal distance between the left and right microstrip lines. Probe 3 is directly under the ground plane of the left line.

The field plots and the conclusions derived from them indicate the elimination of two parasitic modes. To confirm the existence of these modes and the effect of the via posts, the effective permittivity and magnitude of the electric field at 25 GHz

at locations shown in Fig. 11 are measured and shown in Table 1. First, note that, qualitatively, the ϵ_{eff} of microstrip lines W1 and W3 shown in Table 1 agree with the measured values shown in Fig. 3. The FDTD analysis did not account for metal loss and therefore the effects of internal inductance on ϵ_{eff} are not included. Thus a quantitative agreement cannot be obtained. Second, the addition of via posts does not change the ϵ_{eff} of the two microstrip modes, which indicates that the microstrip modes are not effected by the via posts. The 3 dB reduction in magnitude of the electric field for probe 2, the coupled microstrip line, with via post is a measure of the reduction in coupling that was presented in Fig. 6a. The mode detected by probe 3 has an ϵ_{eff} greater than the ϵ_r of the polyimide, which indicates a mode that propagates in the silicon wafer and the polyimide below the ground plane. The via post reduces the magnitude of this mode by approximately 10 dB. In addition, the higher value of its ϵ_{eff} for the via-enabled geometry indicates that in this case, most of this mode is eliminated from the via-shielded lower ϵ_r polyimide and is concentrated in the silicon substrate. Because the ϵ_{eff} measured by probe 4 is nearly equal to the ϵ_r of the polyimide, it is surmised that this is a slotline type mode between the two ground planes. This conclusion is supported by the elimination of this mode when the two ground planes are connected by via posts. However, without the via posts, this slotline mode is stronger than the microstrip mode in the coupled microstrip line. Other modes have magnitudes too small to influence the characteristics.

VI. CONCLUSION

In this paper, theoretical analysis and measured characteristics show that parallel, thin film microstrip lines with finite width ground planes support and excite multiple modes, which degrades the isolation between the lines. By interconnecting the two ground planes with via posts, two of these parasitic modes are reduced or eliminated. One of the modes is a dielectric waveguide type mode that the via posts reduce by 10 dB. The other is a slotline type mode that is very strongly excited in the coupled lines without via posts. These results show that if finite width ground plane microstrip lines are used for 3D-MMICs and thin film packages, it is advisable to connect the ground planes periodically with metal filled via posts and to use a wider ground plane width for higher isolation. Although these conclusions are based on experimental and theoretical analysis of thin film polyimide layers on silicon, they may be extended to other 3D circuits and packaging structures that include multiple materials.

Acknowledgments

The authors wish to acknowledge the support of the Georgia Tech NSF Packaging Research Center, The Yamacraw Design Center of the State of Georgia, NSF CAREER Grant# 9984761, NSF SGER Grant# 0196376 and NASA Award #NAG3-2329.

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Table 1: Effective permittivity and magnitude of modes measured at probe points shown in Fig. 11.

Probe and mode type	Effective permittivity		Magnitude (dB)	
	No via	Via post	No via post	Via post
1, microstrip (W1)	2.89	2.90	0	0
2, microstrip (W3)	2.73	2.70	-27.5	-30.2
3, dielectric waveguide	4.54	6.93	-31.2	-42.0
4, slotline	2.92	-	-19.7	-